IN THE CLAIMS:

Please AMEND the claims as indicated below and ADD the new claims also as listed below:

Listing of the Claims

1. (CURRENTLY AMENDED) A semiconductor package obtained by collectively fabricating a plurality of semiconductor packages on a wafer in a batch process producing a wafer product and dicing the wafer product into discrete semiconductor packages, wherein:

said semiconductor package is a stacked body formed by bonding two or more semiconductor devices through an insulating layer;

each of said semiconductor devices comprises a substrate and a device pattern formed on a surface thereof; and

a device pattern surface of a lower semiconductor device faces a non-device pattern surface of a semiconductor device stacked on said lower semiconductor device, wherein

said semiconductor device positioned, in sequence, as a lowermost semiconductor device and further comprising a back surface protective film, and a heat radiation layer of a material having a high heat transfer rate, on the non-device pattern surface of the lowermost semiconductor device, and

said back surface protective film is bonded to a back surface of the stacked body by bonding an insulating epoxy resin film to form the back surface protective film.

2. (CANCELLED)

3. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is deposited on the non-device pattern surface of a wafer as the lowermost layer, before said semiconductor packages are diced.

4. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is one formed by a thin film formation technology.

5. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is made of copper, aluminum or an alloy.

6. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer also acts as a support.

7. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said insulating layer comprises a polyimide resin or an epoxy resin.

8. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said semiconductor device positioned as the uppermost layer further comprises a resin sealing layer on the device pattern surface thereof, and said resin sealing layer is one formed on the device pattern surface of the wafer as the uppermost layer, before said semiconductor package is diced.

9. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein the device patterns of said semiconductor devices stacked are electrically connected to one another through a re-wiring layer and a substrate through-electrode that are simultaneously formed in one semiconductor device.

10. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 9, wherein each of said re-wiring layer and said substrate through-electrode is formed of copper or its alloy.

11. – 18. (CANCELLED)

19. (NEW) A semiconductor package comprising:

a layered stack of two or more semiconductor devices, wherein each semiconductor device layer comprises:

a substrate and a non-device pattern surface formed on one side of the substrate and a non-device pattern surface formed on an opposing side of the substrate;

an insulator bonding layer interposed between the non-device pattern surface of one semiconductor layer and the device pattern surface of an adjacent semiconductor layer;

an epoxy resin protective film bonded to the non-device pattern surface of the lowermost semiconductor layer of the stack; and

a heat radiation layer bonded to the electrically insulating layer, wherein the heat radiation layer has a thickness from about 0.1μm to about 1μm.

20. (NEW) The semiconductor package of claim 19, wherein the thickness of the heat radiation layer is from about 0.1μm to about 0.5μm and wherein the epoxy resin is electrically insulating.

21. (NEW) The semiconductor package of claim 19, wherein the layered stack is a diced stack.

22. (NEW) The semiconductor package of claim 19, wherein the heat radiation layer comprises Cu, Al or an alloy thereof.

23. (NEW) The semiconductor package of claim 22, wherein the heat radiation layer comprises Cu or an alloy thereof.

24. (NEW) The semiconductor package of claim 22, wherein the heat radiation layer consists essentially of Cu, Al or an alloy thereof.

25. (NEW) The semiconductor package of claim 24, wherein the heat radiation layer consists essentially of Cu or an alloy thereof.

26. (NEW) The semiconductor package of claim 24, wherein the heat radiation layer consists of Cu, Al or an alloy thereof.

27. (NEW) The semiconductor package of claim 19, wherein the insulating layer comprises an epoxy resin or a polyimide resin.

28. (NEW) The semiconductor package of claim 27, wherein the insulating layer comprises an epoxy resin.

29. (NEW) The semiconductor package of claim 27, wherein the insulating layer comprises an electrically insulating epoxy resin.

30. (NEW) The semiconductor package of claim 19 further comprising:

a resin sealing layer bonded on the device pattern surface of an uppermost semiconductor device layer.

31. (NEW) The semiconductor package of claim 19, wherein the layered stack is diced.

32. (NEW) The semiconductor package of claim 19, wherein each semiconductor device layer comprises an electrode pad formed as part of the device pattern surface of each layer and the electrode pads of successive semiconductor device layers are connected by a via electrode between the electrode pads.

33. (NEW) The semiconductor package of claim 32, wherein the electrode pads and the via electrodes between them comprise Cu or an alloy thereof.

34. (NEW) The semiconductor package of claim 30, wherein the resin sealing layer has a thickness from about 50μm to about 90μm.

35. (NEW) The semiconductor package of claim 30, wherein the resin sealing layer has a thickness from about 60μm to about 80μm.

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